(19) JAPANESE PATENT OFFICE (JP)

(12) KOKAI TOKUHYO PATENT JOURNAL (X)

(11) PATENT APPLICATION PUBLICATION
NO. HEI 11[1999]-177653
(43) Publication Date: July 2, 1999

| (51) Int. Cl.[6]: | Identification Codes: | FI | |
|---|---|---|---|
| H04L 29/08 | | H04L 13/00 | 307C |
| H04N 7/24 | | H04N 7/13 | Z |

Examination Request: Not filed

No. of Claims: 3 (Total of 8 pages)

(21) Filing No.: Hei 9[1997]-339131

(22) Filing Date: December 9, 1997

(71) Applicant: 00004237
NEC Corp.
5-7-1 Shiba, Minato-ku, Tokyo

(72) Inventor: Yukihiro Tanaka
NEC Corp.
5-7-1 Shiba, Minato-ku, Tokyo

(74) Agents: Tsuguo Takahashi, patent attorney, and 4 others

(54) [Title] MPEG data transfer control circuit

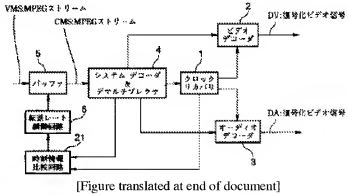
(57) Abstract

Objective

The objective is to receive a stable MPEG stream in synchronization with the clock on the transmission side without generating a large deviation in the reference clock of the decoder system on the reception side even if the jitter in the received MPEG stream increases abruptly.

Means to solve

The received MPEG data are stored in buffer 5. Transfer rate control circuit 6 transfers the MPEG data accumulated in buffer 5 at a constant transfer rate to system decoder & demultiplexer 4. Time information comparison circuit 21 compares the time information included in the MPEG data read out from buffer 5 with the time indicated by the reference clock used for timing control of the decoder in system decoder & demultiplexer 4 and sends a command for changing the transfer rate to transfer rate control circuit 6 based on the comparison result.




[Figure translated at end of document]

There are no amendments to this patent.

Claims

1. An MPEG data transfer control circuit, characterized by having a buffer that sequentially accumulates the received MPEG data,

a transfer rate control circuit that transfers the MPEG data stored in said buffer at a constant transfer rate to a decoder, and

a time information comparison circuit that compares the time information included in the MPEG data read out from said buffer with the time indicated by the reference clock used for timing control of said decoder and sends a command for changing the transfer rate to the transfer rate control circuit based on the comparison result.

2. The MPEG data transfer control circuit described in Claim 1, characterized by the fact that said time information comparison circuit sends a command for raising said transfer rate or a command for lowering said transfer rate to the transfer rate control circuit when the difference between the time information included in the packets read out from the buffer and the time indicated by the reference clock used for timing control of said decoder is equal to or bigger than a prescribed value.

3. The MPEG data transfer control circuit described in Claim 1, characterized by the fact that said time information comparison circuit periodically writes the difference between the time information included in the packets read out from the buffer and the time indicated by the reference clock used for timing control of said decoder into a time information storage circuit, determines the rate for raising or lowering the transfer rate corresponding to the timing variation of each difference stored in the time information storage circuit, and sends a command for raising or lowering the transfer rate to the transfer rate control circuit in accordance with the determination result.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention relates to an MPEG decoder, particularly, to an MPEG data transfer control circuit used for supplying the MPEG data received via a transmission path at a constant rate to a decoder.

[0002]

Prior art

The MPEG (moving picture experts group) specification (ISO/IEC DIS 11172/13818) used commonly in the fields of storage media, communication, broadcasting, and the like is an international standard specification for digital moving picture (video) coding (compression),

sound (audio) coding, and multiplexing/demultiplexing systems thereof. As far as the MPEG specification is concerned, in addition to MPEG1 used for CD-ROM (compact disk - read only memory) or other storage media and the applications of MPEG1, there is MPEG2 used in a wide range of applications in the broadcast and communication fields. Like MPEG1, MPEG2 also has two forms, that is, MPEG2 program stream (PS) that can constitute one program in stream and MPEG2 transport stream (TS) that can constitute a plurality of programs in stream. In particular, since MPEG2-TS can combine a plurality of programs in one stream, it can also be used for TV broadcasts or the like. MPEG2-TS also allows the freedom of program editing or a scramble function or the like in order to exploit the aforementioned advantage.

[0003]

In the following, an MPEG system that performs data transmission corresponding to MPEG as explained above will be discussed. In this MPEG system, the digitized video signals and audio signals are compressed on the transmission side and are transferred to the reception side through a network, hard disk, or other medium. Then, the original video signals and audio signals are recovered from the compressed data on the reception side. In this case, the encoding system of MPEG adopts irreversible encoding in order to reduce the information amount as much as possible. Therefore, the original video signals and audio signals cannot be fully recovered on the reception side. The MPEG encoding system cleverly takes advantage of the weakness in the sense of vision and sense of hearing of human being and reduces the information amount to such a degree that is barely noticeable to the human being. However, when the transfer rate of the MPEG data drops (that is, when the information amount is reduced), the difference from the original picture, original sound that can be noticed by human beings is increased. The MPEG system has been explained above.

[0004]

Figure 4 is a block diagram illustrating the basic configuration of the MPEG system explained above. Figure 5 is a block diagram illustrating a configuration example of the decoder system in the MPEG system. Figure 6 is a block diagram illustrating the configuration of the clock recovery in decoder system 9.

[0005]

In Figure 4, MPEG encoder system 7 includes encoder, buffer, clock control circuit, and the like. Video VI as the video signal and audio input AI as the audio signal are input into encoder system 7. Then, MPEG encoder system 7 compressed the input information and outputs the compressed (MPEG encoded) MPEG stream. The MPEG stream is input into MPEG decoder

system 9 through a network or video server 8. MPEG decoder system 9 decodes the compressed stream and outputs video output VO and audio output AO.

[0006]

In this MPEG system, however, the signal transfer between the input terminal of MPEG encoder system 7 and the output terminal of MPEG decoder system 9 must be always performed with a constant delay. This is because the video signals or the audio signals must be transferred in real time in the original waveform in the MPEG system. For example, for the video or audio signals input into encoder system 7, the signals input exactly 1 sec, 2 sec, 3 sec ... from the starting input time point of the head signal must be output exactly 1 sec, 2 sec, 3 sec ... from the starting output time point of the head signal when they are output from decoder system 9.

[0007]

Also, in the MPEG system, the signal transfer between the output terminal of encoder system 7 and the input terminal of decoder system 9 must also be performed with constant delay. The reason is as follows. In the MPEG system, encoder system 7 includes the time information indicating the timing of the clock on the encoder side (the time information intended by the encoder) in the transferred MPEG stream. When the time information is received by decoder system 9, the reference clock used for controlling the reproduction and output timing of the video and audio is synchronized with the clock on the encoder side (the synchronization control will be explained later). Consequently, if the delay of the signal transfer between the output terminal of encoder system 7 and the input terminal of decoder system 9 is not constant, the reception timing of the time information in decoder system 9 becomes scattered, and the reference clock on the decoder side deviates from the clock on the encoder side. In addition, if the delay of the signal transfer between the output terminal of encoder system 7 and the input terminal of decoder system 9 is not constant, it is unable to transfer signals between the input terminal of MPEG encoder system 7 and the output terminal of MPEG decoder system 9 with a constant delay. Therefore, it is necessary to transfer signals between the output terminal of encoder system 7 and the input terminal of decoder system 9 with a constant delay as described above.

[0008]

In fact, the MPEG stream is transferred via the bus of a network or computer system. Therefore, it is difficult to keep the delays at the output terminal of encoder system 7 and the input terminal of decoder system 9 constant. In the following, this problem will be explained with reference to Figure 7.

[0009]

Figure 7 shows an example of the relationship between the expected value of the data arrival time when an MPEG stream is input into a decoder and the actual arrival time in the MPEG system. In this case, the MPEG stream output from the encoder is transferred in a coherent unit (like cell in ATM: fixed length) at a certain interval. Under this prerequisite, if the delay on the path until the MPEG stream is input into the decoder is always constant, the arrival time of the cell becomes constant as shown in Figure 7(a). In fact, however, transfer of the MPEG stream is affected by various factors (congestion of the network, congestion of the bus inside the video server, data reading time from the hard disk). Therefore, the arrival time of the cell deviates from the expected time as shown in Figure 7(b). The fact that the arrival time of each cell becomes scattered is known as jitter (jitter).

[0010]

Since jitter occurs during transfer of MPEG stream as described above, it would be difficult to recover the time information correctly on the reception side without taking any measures. Therefore, a means used for eliminating jitter is provided in the decoder system on the reception side in the MPEG system. In the following, the configuration of the means will be explained with reference to Figure 5.

[0011]

In the decoder system shown in Figure 5, in order to eliminate the jitter, a buffer 5 is provided before system decoder & demultiplexer 4 used for extracting the time information from the MPEG stream. The MPEG stream VMS (VMS: variable delay MPEG stream) including the jitter is temporarily stored in buffer 5. Then, the MPEG stream accumulated in buffer 5 is read out at a constant rate by transfer rate control circuit 6 to become MPEG stream CMS (CMS: constant delay MPEG stream) with constant transfer rate containing no jitter. The transfer rate for the MPEG stream is preset in transfer rate control circuit 6.

[0012]

System decoder & demultiplexer separates the MPEG stream CMS into video and audio packets and outputs these packets to video decoder 2 and audio decoder 3, respectively. Video decoder 2 decodes the received video packets and outputs video signals DV. Similarly, audio decoder 3 decodes the received audio packets and outputs audio signals DA.

[0013]

Since video signals DV and audio signals DA are decoded separately, if the decoded data are directly output, the reproduction times of these signals may be different from the expected ones. For example, in the case of reproducing the MPEG data of a scene when people are talking, the movement of the mouth may not match the voice. Therefore, for MPEG, the reproduction time management information (PTS: presentation time stamp) for video and audio are included in the respective packets, and the data of the packets are reproduced and output when the reference clock (STC: system time clock) possessed by the decoder system in each decoder matches the PTS.

[0014]

In this case, the STC on the decoder side must be correctly consistent with the time reference clock on the encoder side. However, even if the same kind of oscillator produced by the same manufacturer is used on both the encoder side and the decoder side, some kind of error may be present between the clocks because two oscillators are used. Consequently, even if the two clocks are almost synchronized and there is only slight discrepancy that is unnoticeable to the eye at the beginning, when the MPEG data are reproduced over long term, the discrepancy will increase, and the movement on the screen becomes mismatched with the voice.

[0015]

In order to correct this discrepancy, the time information on the encoder side (in MPEG1, MPEG2 program stream, SCR: system clock reference, in MPEG2 transport stream, PCR: program clock reference) is periodically included in the MPEG stream (see Figures 8, 9). The value of the SCR or PCR on the decoder side, that is, the value intended on the encoder side is set to STC. In this case, accuracy of the arrival time of the MPEG stream input on the decoder side is required.

[0016]

The configuration example of clock recovery circuit 1 shown in Figure 6 comprises STC and PLL (phase locked loop; a feedback enclosed circuit comprising phase comparator 13, lowpass filter 14, and voltage controlled oscillator (VCXO: voltage-controlled crystal oscillator) 11). This circuit can delicately correct the deviation of STC so that the decoder can have an STC with a completely consistent frequency with the system clock on the encoder side.

[0017]

The details of the MPEG system explained above can be found, for example, in ISO/IEC DIS 11172-1 and ISO/IEC DIS 13818-1.

[0018]

Problem to be solved by the invention

However, the aforementioned conventional MPEG system has the following problem. That is, the capacity of buffer 5 provided in decoder system 9 is determined in consideration of the jitter of the MPEG stream VMS predicted beforehand. However, when the jitter increases abruptly due to some reason, it may be unable to absorb the jitter due to the capacity of buffer 5. When this happens, a disturbance may occur in the picture or sound during reproduction of video or audio of MPEG. This is because the range of the clock frequency that can be adjusted by VCXO 11 of clock recovery circuit 1 is very narrow.

[0019]

The objective of the present invention is to solve the aforementioned problem by providing an MPEG data transfer control circuit that can receive a stable MPEG stream in synchronization with the clock on the transmission side without generating large deviations in the reference clock of the decoder system on the reception side even if the jitter in the received MPEG stream increases abruptly.

[0020]

Means to solve the problem

The present invention provides an MPEG data transfer control circuit, characterized by having a buffer that sequentially accumulates the received MPEG data, a transfer rate control circuit that transfers the MPEG data stored in said buffer at a constant transfer rate to a decoder, and a time information comparison circuit that compares the time information included in the MPEG data read out from said buffer with the time indicated by the reference clock used for timing control of said decoder and sends a command for changing the transfer rate to the transfer rate control circuit based on the comparison result.

[0021]

Embodiment of the invention

In the following, the embodiment of the present invention will be explained with reference to the figures.

[0022]

A. First embodiment

Figure 1 is a block diagram illustrating the configuration of the MPEG decoder system to which the MPEG data transfer control circuit disclosed in an embodiment of the present invention is applied. This MPEG decoder system is incorporated in a personal computer or the like. It can reproduce MPEG files stored in a hard disk or the like.

[0023]

In Figure 1, buffer 5 is a means that accumulates the MPEG stream VMS transferred from an encoder via a transmission path. In this case, the MPEG stream VMS transferred via the transmission path usually includes jitter. The data accumulated in buffer 5 are read out at a prescribed transfer rate under the control of transfer rate control circuit 6 and become MPEG stream CMS, which is supplied to system decoder & demultiplexer 4.

[0024]

Said system decoder & demultiplexer 4 analyzes the MPEG stream CMS. The video packets in the MPEG stream CMS are transferred to video decoder 2, and the audio packets are transferred to audio decoder 3. Also, system decoder & demultiplexer 4 extracts the SCR or PCR from the MPEG stream CMS and provides it to clock recovery circuit 1 and time information comparison circuit 21.

[0025]

Clock recovery circuit 1 correctly matches the STC used as the reference clock of the MPEG data system obtained from the SCR or PCR extracted by system decoder & demultiplexer 4. In this case, the controlled STC is connected to video decoder 2, audio decoder 3, and time information comparison circuit 21.

[0026]

Video decoder 2 decodes the video packets extracted by system decoder & demultiplexer 4 and outputs video signals DV. Decoding of the video packets and output of the video signals DV by said video decoder 2 are carried out in synchronization with the audio signals in accordance with the STC in clock recovery circuit 1. On the other hand, audio decoder 3 decodes the audio packets extracted by system decoder & demultiplexer 4 and outputs audio signals DA. Decoding of the audio packets and output of audio signals DA by said audio decoder 3 are carried out in synchronization with the video signals in accordance with the STC in clock recovery circuit 1.

[0027]

Time information comparison circuit 21 compares SCR or PCR with STC and sends the result to transfer rate control circuit 6. Transfer rate control circuit 6 is connected to buffer 5. The MPEG system CMS is transferred from buffer 5 to system decoder & demultiplexer 4 at a preset transfer rate. The transfer rate, however, can be changed based on the information sent from transfer rate control circuit 6.

[0028]

In the following, the operation of this embodiment will be explained. In Figure 1, the MPEG stream VMS input into buffer 5 is slightly delayed and does not keep up with the transfer rate of the MPEG stream CMS output from buffer 5. In this case, the MPEG stream accumulates in buffer 5 is gradually reduced, and buffer 5 becomes empty. At that time, STC is corrected to the value intended on the encoder side by using the SCR or PCR obtained so far. After that, the MPEG stream VMS is input into buffer 5 starting from the empty state of buffer 5. The MPEG stream CMS is transferred from buffer 5. When the packets including SCR or PCR are input into system decoder & demultiplexer 4, the SCR or PCR becomes a value that significantly deviates from STC.

[0029]

In this embodiment, the SCR or PCR is compared with STC at that time using time information comparison circuit 21, and the transfer rate of the MPEG stream CMS output from buffer 5 is changed under the control of the transfer rate control circuit depending on the magnitude of the difference. In this way, it is possible to quickly recover the difference between the SCR or PCR and STC that exceeds the range recoverable by clock recovery circuit 1.

[0030]

Figure 2 is a time chart illustrating the relationship between the transfer state of the MPEG stream and the time information in this embodiment. In the following, the operation of this embodiment will be explained in detail with reference to Figure 2. In Figure 2, buffer Empty indicates the state when buffer 5 is empty. VMS represents the period during which MPEG stream VMS is transferred to buffer 5. CMS represents the period during which MPEG stream CMS is transferred from buffer 5 to system decoder & demultiplexer 4. The thick line part means that the data are transferred at a higher rate than the normal transfer rate. STC represents the STC in the MPEG decoder system. SCR/PCR represents the SCR/PCT extracted by system decoder &

demultiplexer 4. The time information is described in simple integers for convenience. It is different from the time information that is actually handled.

[0031]

Under normal circumstances, MPEG stream VMS is read into buffer 5 under such management that buffer 5 does not become empty. When MPEG stream VMS into buffer 5 is such that buffer 5 becomes full, transfer of MPEG stream VMS is stopped. MPEG stream CMS reads out the data stored in buffer 5 to continue the transfer. When buffer 5 is close to the empty state, transfer of MPEG VMS is started again. This operation is carried out repeatedly so that MPEG CMS is transferred continuously.

[0032]

Now, let us consider a case in which transfer of MPEG stream VMS is stopped for some reason and all of the data in buffer 5 have been cleaned out. When there is no data in buffer 5, MPEG stream CMS is not transferred. At that time, STC continuously records time every certain period. When transfer of MPEG stream VMS is restarted, since there are data stored in buffer 5, transfer of MPEG stream CMS is started again. System decoder & demultiplexer 4 detects SCR or PCR. However, the detected SCR or PCR should match the STC immediately after transfer of MPEG stream CMS is cut off and has a value that is significantly different from the STC at that point. For example, SCR/PCR = 6 while STC is slightly over 7.

[0033]

In the case of the conventional technology explained above, STC will be adjusted delicately by clock recovery circuit 1 (in this embodiment, the clock is adjusted in the delayed direction) so that STC gradually becomes the same value as SCR or PCR.

[0034]

On the other hand, in this embodiment, it is detected by time information comparison circuit 21 that there is a large difference between STC and SCR or PCR. If it is found that STC advances (that is, has bigger value) ahead of SCR or PCR, time information comparison circuit 21 notifies transfer rate control circuit 6 of that fact. The transfer rate is controlled until the value of SCR or PCR almost catches up with the value of STC. The time required for this adjustment is very short compared with that of the conventional method.

[0035]

As far as the reproduction of video and audio in that period is concerned, the data left in system decoder & demultiplexer 4 as well as video decoder 2 and audio decoder 3 before that are reproduced. That is, a memory is actually connected to the circuit constituting the system decoder & demultiplexer. Several packets of MPEG stream CMS prepared for transfer to each decoder are left in the memory of system decoder & demultiplexer 4. The packets prior to decoding and the data prepared for output (several frames of image data in the case of video decoder 2) are left in the memory of each decoder. Consequently, the aforementioned remaining data can be reproduced during the aforementioned period.

[0036]

The case in which the value of SCR and PCR is delayed with respect to the value of STC has been explained above. On the other hand, when the value of SCR or PCR advances with respect to the value of STC, transfer rate control circuit 6 operates to delay the transfer rate of the MPEG stream CMS.

[0037]

The embodiment explained above can realize the following effects.

(1) When SCR or PCR is significantly delayed compared with STC, MPEG stream CMS is transferred at a high speed until the difference is almost eliminated. Therefore, the value of SCR or PCR can quickly catch up with STC.

(2) Since the value of SCR or PCR can quickly catch up with STC as described above, the period in which the period of STC is disturbed becomes short. Consequently, delay in the picture or sound being reproduced becomes unnoticeable.

[0038]

B. Second embodiment

Figure 3 is a block diagram illustrating the configuration of the second embodiment of the present invention. In this embodiment, a time information storage circuit 22 is connected to time information comparison circuit 21 in the aforementioned first embodiment (Figure 1). The result (difference information) of comparing STC with the SCR or PCR extracted by system decoder & demultiplexer 4 is exchanged between time information comparison circuit 21 and said time information storage circuit 22. This will be explained in detail below.

[0039]

First, time information comparison circuit 21 constantly compares SCR or PCR with STC and writes the comparison result, that is, the difference information between the time indicated by SCR or PCR and the time indicated by STC periodically (for example, when STC changes) into time information storage circuit 22. Also, when time information comparison circuit 21 compares SCR or PCR with STC, it reads out the difference information of the time written previously into time information storage circuit 22.

[0040]

Time information comparison circuit 21 compares the difference information at the current time with the previous difference information to determine whether the value of the current SCR or PCR is delayed or advanced compared with STC. The delay can be found by comparing the comparison results of several rounds in the past, and it is possible to tell based on the difference condition how many percent the transfer rate of the current MPEG stream CMS should be advanced. Therefore, the transfer rate of the MPEG stream CMS is set earlier by that percentage with respect to transfer rate control circuit 6. Since the MPEG stream CMS is transferred at the transfer rate newly set in transfer rate control circuit 6, the difference between SCR or PCR and STC that has been gradually increased so far will not be further increased compared with the previous state. Similarly, when SCR or PCR is ahead of STC, time information comparison circuit 21 can set the transfer rate appropriately so that the transfer rate of MPEG stream CMS is delayed with respect to transfer rate control circuit 6. Whether the difference information of the time between SCR or PCR and STC in the past leads or lags, time information comparison circuit 21 will not set new transfer rate with respect to transfer rate control circuit 6.

[0041]

Effect of the invention

As explained above, by using the MPEG data transfer control circuit disclosed in the present invention, even if the jitter of the received MPEG stream increases abruptly, it is still able to receive a stable MPEG stream in synchronization with the clock on the transmission side without generating significant deviation in the reference clock of the decoder system on the reception side.

Brief description of the figures

Figure 1 is a block diagram illustrating the configuration of an MPEG decoder system to which the MPEG data transfer control circuit disclosed in an embodiment of the present invention is applied.

Figure 2 is a time chart illustrating the operation in this embodiment in comparison with the prior art.

Figure 3 is a block diagram illustrating the configuration of an MPEG decoder system to which the MPEG data transfer control circuit disclosed in the second embodiment of the present invention is applied.

Figure 4 is a block diagram illustrating the configuration of a general MPEG system.

Figure 5 is a block diagram illustrating the configuration of a conventional MPEG decoder system.

Figure 6 is a block diagram illustrating an example of the configuration of the conventional clock recovery circuit in the conventional MPEG decoder system.

Figure 7 is a diagram illustrating an example of the transmission form of a cell in the MPEG system.

Figure 8 is a diagram illustrating an example of the program stream in the MPEG system.

Figure 9 is a diagram illustrating an example of transport stream in the MPEG system.

Explanation of the reference symbols

5 Buffer
6 Transfer rate control circuit
21 Time information comparison circuit
4 System decoder & demultiplexer
1 Clock recovery
2 Video decoder
3 Audio decoder
22 Time information storage circuit

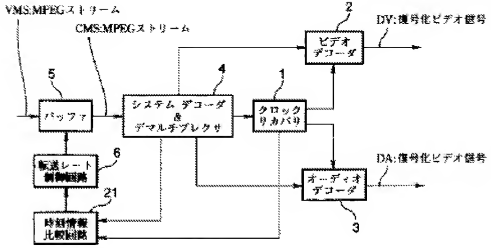



Figure 1

Key:
VMS: MPEG stream
CMS: MPEG stream
DV: Decoded video signal
DA: Decoded video signal
1 Clock recovery
2 Video decoder
3 Audio decoder
4 System decoder & demultiplexer
5 Buffer
6 Transfer rate control circuit
21 Time information comparison circuit

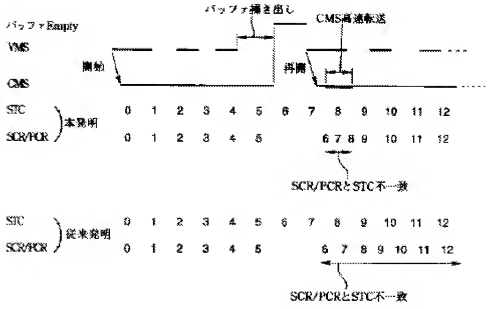



Figure 2

Key
1 Buffer Empty
2 Sweep out the buffer
3 High-speed transfer of CMS
4 Start
5 Restart
6 Present invention
7 Prior art
8 SCR/PCR is inconsistent with STC

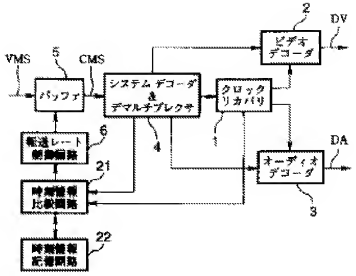



Figure 3

Key
1 Clock recovery
2 Video decoder
3 Audio decoder
4 system decoder & demultiplexer
5 Buffer
6 Transfer rate control circuit
21 Time information comparison circuit
22 Time information storage circuit

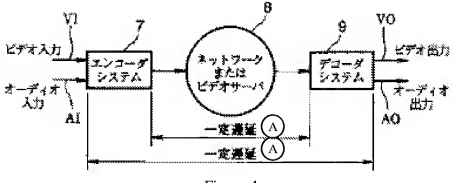



Figure 4

Key
7 Encoder system
8 Network or video server
9 Decoder system
A Certain delay
AI Audio input

AO Audio output
VO Video output
VI Video input

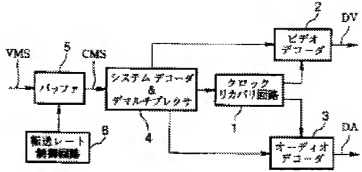



Figure 5

Key 1 Clock recovery
2 Video decoder
3 Audio decoder
4 System decoder & demultiplexer
5 Buffer
6 Transfer rate control circuit

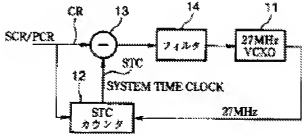



Figure 6

Key 14 Filter
12 STC counter

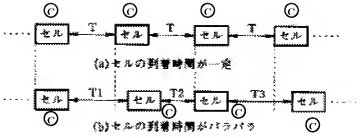



Figure 7

Key (a) The arrival time of the cell is constant
(b) The arrival time of the cell is scattered
C Cell

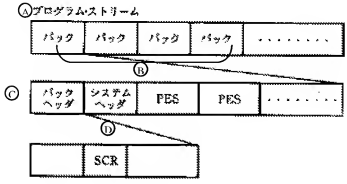



Figure 8

Key A Program stream
B Pack
C Pack header
D System header

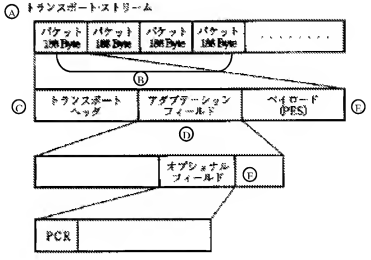



Figure 9

Key A Transport stream
B Packet
C Transport header
D Adaptation filed
E Payload (PES)
F Optional field